REMARKS

This is a full and timely response to the non-final Office Action (Paper No. 2) mailed by the U.S. Patent and Trademark Office on January 7, 2002. Upon entry of the foregoing amendments, claims 1-26 remain pending in the present application. Claims 1, 6, 9, 10, 11, 14 and 15 have been amended, and new dependent claims 16-26 have been added, to define further the present invention. It is believed that the foregoing amendments and additions add no new matter to the present application. In view of the foregoing amendments and the following remarks, reconsideration and allowance of the present application and pending claims are respectfully requested.

Rejections Under 35 U.S.C. § 102(e)

The Office Action rejected claims 1-4, 6-8, and 11-13 under 35 U.S.C. § 102(e) as allegedly "being anticipated by *McMahan* et al. U.S. Patent no. 5,870,446." Office Action, p. 2 (italics added). For a proper rejection of a claim under 35 U.S.C. § 102(e), the cited reference must disclose all elements/features/steps of the claim. *See, e.g., E.I. du Pont de Nemours & Co. v. Phillips Petroleum Co.*, 849 F.2d 1430, 7 USPQ2d 1129 (Fed. Cir. 1988).

As amended herein, independent claim 1 provides as follows:

> 1. A circuit for detecting errors in the synchronization of a DTE (data terminal equipment) data signal with a DCE (data communication equipment) clocking signal, in a communication environment wherein the DCE interfaces the DTE to a communication channel at an interface rate determined by the DCE clocking signal, the circuit comprising:
>
> a master clock producing a master clock signal having a frequency greater than the frequency of the DCE clocking signal;
>
> ***a clock generator deriving a circuit clocking signal from said master clock signal***, said circuit clocking signal having the same frequency as the DCE clocking signal;

a sample enable generator for generating a first sample enable signal at a first time and a second sample enable signal at a second time; and

a sample comparator for using said first sample enable signal, said second enable signal and said DTE data signal to determine whether the DTE data signal has undergone a transition during the time interval between said first time and said second time.

(emphasis added).[1]

The Office Action based its section 102(e) rejection of claim 1 on its characterization of *McMahan*, as follows:

Regarding claim 1, McMahan et al. shows in figure 1, a circuit for detecting errors in the synchronization of a DTE date signal (11) with a DCE clocking signal (43 and 55) in a communication environment wherein the DCE interfaces the DTE to a communication channel at an interface rate determined by the DCE clocking signal (43 and 55), the circuit comprising:

a. a master clock producing a master clock signal (HS CLK) having a frequency greater than the frequency of the DCE clocking signal. At the end of the first full paragraph of column 6, it is implied that the master clock signal is 16MHz and the DCE clocking signal is 1.544 MHz;

b. ***a clock generator (55) deriving a circuit clocking signal from said master clock signal (HS CLK input to 48)***, said clocking signal having the same frequency as the DCE clocking signal;

c. a sample enable generator (15) for generating a first sample enable signal at a first time and a second sample enable signal at a second time; and

d. a sample comparator (21) for using said first sample enable signal and said second enable signal to obtain a first sample of said DTE date signal (11) at said first time and a second sample of said DTE data signal at said second time, and for determining whether the DTE data signal (11) has undergone a transition (21) during the time interval between said first time and said second time.

Office Action, pp. 2-3 (emphasis added).

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[1] The amendment to claim 1 was made to define further the sample comparator element. The amendment to claim 1 made no change to the clock generator element.

The Office Action states that *McMahan* shows "a clock generator (55) deriving a circuit clocking signal from said master clock signal (HS CLK input to 48)." However, Applicants respectfully submit that while *McMahan* appears to show two signals having different frequencies, the signals disclosed in *McMahan* do not anticipate the emphasized element of claim 1, namely ***"a clock generator deriving a circuit clocking signal from said master clock signal."*** There is no disclosure, teaching or suggestion in *McMahan* that the clock generator (55) ***derives*** a clocking signal ***from*** the master clock signal (HS CLK input to 48).

McMahan appears to disclose that the HS CLK signal is used to clock the timing window shift register 41, and the output 35 of the timing window shift register 41 is used to delay the TX edge of the TX CLK signal. However, there is nothing in *McMahan*'s disclosure to indicate that the TX CLOCK signal at the output of TX CLOCK GENERATOR 55 is ***derived*** from the HS CLK signal. The HS CLK signal is not an input to TX CLOCK GENERATOR 55, and there is nothing in the description or drawings to indicate that the TX CLOCK signal is ***derived*** from the HS CLK.

To the contrary, *McMahan* makes clear that the HS CLK and the TX CLOCK are separate and distinct clocks. As acknowledged in the Office Action, *McMahan* indicates that the HS CLK signal has a frequency of 16MHz, while the TX CLOCK signal has a frequency of 1.544 MHz. *See* Office Action, p. 2, ¶3a; *McMahan*, col. 6, lines 19-21. Thus, because 16MHz is not an integral multiple of 1.544MHz, it is clear that the HS CLK signal and TX CLOCK signal are separate signals and that the TX CLOCK signal is ***not derived from*** the HS CLK signal.

In contrast, claim 1 of the present application requires "a clock generator ***deriving*** a circuit clocking signal ***from*** said master clock signal." This is confirmed by the alternative embodiments described in the specification with regard to FIGS. 4 and 5. In each alternative embodiment, the output of the master clock 31 is input to clock generator 32, and the circuit clocking signal is thereby derived from the master clock signal.

For the same reasons, *McMahan* likewise fails to teach, suggest or disclose all of the elements/steps/features of amended independent claims 6 and 11. Specifically, *McMahan* fails to teach, suggest or disclose at least the following element of independent claim 6: **"means for deriving a circuit clocking signal from said master clock signal."** Likewise, *McMahan* fails to teach, suggest or disclose at least the following step of independent claim 11: **"deriving a circuit clocking signal from said master clock signal."**

Therefore, *McMahan* does not teach, suggest or disclose all of the elements/features/steps of independent claims 1, 6 and 11, and the section 102(e) rejections of these claims should be withdrawn. *See, e.g., E.I. du Pont de Nemours & Co., supra.*

Furthermore, Applicants respectfully submit that dependent claims 2-5, 7-10 and 12-15, and new claims 16-26, which depend either directly or indirectly from independent claims 1, 6 and 11, respectively, are allowable for at least the reason that they depend from allowable independent claims. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988).

Rejections Under 35 U.S.C. § 103(a)

The Office Action rejected claims 5, 9-10 and 14-15 under 35 U.S.C. § 103(a) as allegedly being unpatentable over *McMahan* in view of U.S. Patent No. 5,470,455 to *Hata*. Office Action, pp. 6-7 (italics added).

"The PTO has the burden under section 103 to establish a *prima facie* case of obviousness. It can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references." *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988) (citations omitted).

A claim cannot be deemed obvious in view of a reference or proposed combination of references if the references "teach away" from the claim. *See In re Gurley,* 2 F.3d 551, 31 USPQ2d 1130, 1131 (Fed Cir. 1994) ("A reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant. ... in general, a reference will teach away if it suggests that the line of development flowing from the reference's disclosure is unlikely to be productive of the result sought by the applicant.").

Here, the Office Action has attempted to use *Hata* to supply elements in dependent claims 5, 9-10 and 14-15 that are admittedly not disclosed, taught or suggested by *McMahan*. However, in view of the arguments set forth above, it is clear that *McMahan* fails to disclose, teach or suggest at least one element of each of the base independent claims 1, 6 and 11, from which claims 5, 9-10 and 14-15 depend. Therefore, the rejections of claims 5, 9-10 and 14-15 under section 103(a) are moot and claims 5, 9-10 and 14-15 are allowable for at least the reason that they depend from allowable independent claims. *In re Fine*, *supra.*

Moreover, by requiring both a high speed clock and a separate transmission strobe clock, *McMahan* teaches away from the concept of a circuit that has a single clock (*e.g.*, a master clock) from which other clocking signals needed by the circuit are derived (*e.g.*, a

circuit clocking signal), as set forth in independent claims 1, 6 and 11, from which claims 5, 9-10 and 14-15 depend. This constitutes another reason why the rejections of claims 5, 9-10 and 14-15 under section 103(a) should be withdrawn.

Newly added claims 16-26

Additional dependent claims 16-26 have been added herein to further define the invention. No new matter has been added. Support for the newly added claims may be found in the specification at pages 7-12, regarding the various embodiments described with respect to FIGS. 4 and 5. The newly added claims are allowable for at least the reason that they depend from allowable independent claims. *In re Fine*, *supra.*

CONCLUSION

For at least the foregoing reasons, Applicants respectfully request that all outstanding rejections be withdrawn and that all pending claims of this application be allowed to issue. If the Examiner has any comments regarding Applicants' response or intends to dispose of this matter in a manner other than a notice of allowance, Applicants request that the Examiner telephone Applicants' undersigned attorney.

Respectfully submitted,

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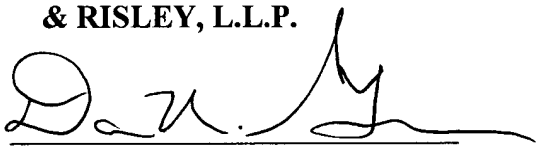
By: 

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ANNOTATED VERSION OF MODIFIED CLAIMS
TO SHOW CHANGES MADE

In accordance with 37 C.F.R. § 1.121, please find below the amended claims in which the inserted language is underlined ("__") and the deleted language is enclosed in brackets ("[ ]"):

1. (Once amended). A circuit for detecting errors in the synchronization of a DTE (data terminal equipment) data signal with a DCE (data communication equipment) clocking signal, in a communication environment wherein the DCE interfaces the DTE to a communication channel at an interface rate determined by the DCE clocking signal, the circuit comprising:

a master clock producing a master clock signal having a frequency greater than the frequency of the DCE clocking signal;

a clock generator deriving a circuit clocking signal from said master clock signal, said circuit clocking signal having the same frequency as the DCE clocking signal;

a sample enable generator for generating a first sample enable signal at a first time and a second sample enable signal at a second time; and

a sample comparator for using said first sample enable signal, [and] said second enable signal and [to obtain a first sample of] said DTE data signal [at said first time and a second sample of said DTE data signal at said second time, and for determining] to determine whether the DTE data signal has undergone a transition during the time interval between said first time and said second time.

6. (Once amended). A circuit for detecting errors in the synchronization of a DTE (data terminal equipment) data signal with a DCE (data communication equipment) clocking signal, in a communication environment wherein the DCE interfaces the DTE to a communication channel, the circuit comprising:

means for producing a master clock signal having a frequency greater than the frequency of the DCE clocking signal;

means for deriving a circuit clocking signal from said master clock signal, said circuit clocking signal having the same frequency as the DCE clocking signal;

means for obtaining a first sample of said DTE data signal at a first time[;] and [means for obtaining] a second sample of said DTE data signal at a second time, said second time being subsequent to said first time, the interval between said first time and said second time being less than the period of the DCE clocking signal; and

means for comparing said first sample to said second sample.

9. (Once amended). The circuit of claim 8, further comprising:

means for [inverting said DCE clocking signal] inverting said circuit clocking signal to produce an inverted circuit clocking signal; and

means for selecting an output signal from the group consisting of said circuit clocking signal and said inverted circuit clocking signal, in response to said selector control signal.

10. (Once amended). The circuit of claim 9, further comprising:

means for [transmitting said inverted DCE clocking signal from said DCE to said DTE in lieu of said DCE clocking signal] latching said DTE data signal.

11. (Once amended). A method for detecting errors in the synchronization of a DTE (data terminal equipment) data signal with a DCE (data communication equipment) clocking signal, in a communication environment wherein the DCE interfaces the DTE to a communication channel, the method comprising the steps of:

providing a master clock signal having a frequency greater than the frequency of the DCE clocking signal;

deriving a circuit clocking signal from said master clock signal, said circuit clocking signal having the same frequency as the DCE clocking signal;

obtaining a first sample of said DTE data signal at a first time and[; obtaining] a second sample of said DTE data signal at a second time, said second time being subsequent to said first time, the interval between said first time and said second time being less than the period of the DCE clocking signal; and

comparing said first sample to said second sample.

14. (Once amended). The method of claim 13, further comprising the steps of:

inverting said circuit clocking signal to produce an inverted circuit clocking signal; and

producing an output signal that is selected from the group consisting of said circuit clocking signal and said inverted circuit clocking signal, [inverting said DCE clocking signal] in response to said selector control signal.

15. (Once amended). The method of claim 14, further comprising the step of:

[transmitting said inverted DCE clocking signal from said DCE to said DTE in lieu of said DCE clocking signal] latching said DTE data signal.